PULSED I-V AND TEMPERATURE MEASUREMENT SYSTEM FOR CHARACTERISATION OF MICROWAVE FETS

R.J.Donarski, A.K.Jastrzebski, J.E.Barnaby

University of Kent at Canterbury
Electronic Engineering Laboratories, Canterbury, Kent CT2 7NT. United Kingdom

ABSTRACT

Systems for pulsed I-V characterisation of GaAs devices must meet specific requirements concerning not just accuracy and pulse width but also the way the measurements are performed and the definition of various quantities which need to be measured in order to acquire a full picture of the device behaviour. Over the last few years such a system has been iteratively developed and tested at the University of Kent at Canterbury. In the light of the experience gained, a number of new measuring concepts together with some vital observations are presented, raising doubts about the validity of currently existing interpretations of pulsed characteristics. Also the design of an inexpensive system incorporating the new concepts is briefly described.

INTRODUCTION

The low frequency dispersion phenomena associated with deep level traps, surface states and temperature are undesirable yet inherent effects in GaAs FETs. These effects can be quantified by utilising a specialised pulsed I-V measurement set-up. Indeed there is a growing interest in using short (i.e. sub-microsecond) pulsed measurements for direct non-linear characterisation of GaAs device behaviour. Such measurements aim to extract data for modelling transient and large signal behaviour. The usual method of acquiring pulsed I-V characteristics involves simultaneous pulsing of both gate and drain from arbitrarily predetermined quiescent potentials and measuring the DUT's current responses to the applied pulse. The essence of present modelling, based on short pulsed measurements, relies on the assumption that the ionisation of traps and the device temperature can not follow the fast change of the voltages so they remain constant at the levels corresponding to the quiescent conditions [3] [5] [8]. Hence, the characteristics obtained in this way can be treated as the instantaneous current and voltage relationship at microwave frequencies for those particular quiescent conditions. Our experiments have shown that with a test pulse of 100 nanosecond duration the thermal effects and most of the trapping effects due to the surface states in the ungated region of the channel [4] [6] remain unchanged. However, at pulsed points corresponding to high electron energies, an almost instantaneous activation of traps takes place with subsequent long release time. This phenomenon shows the limitation of the above modelling assumption and calls for a new approach.

Additionally, accurate information about the temperature at the end of each pulse is required in order to quantify and separate the effects of temperature and the traps. Also, the thermal response characteristic is a vital element for establishing a complete model of the transient and low frequency device behaviour. Techniques for measuring DUT's average temperature, thermal response and the effect of fast activated traps, utilising a specially developed pulse test system, are emphasized.

TH 3F

FAST ACTIVATED DEEP TRAPS

When a 100 nsec duration (20 nsec risetime) voltage test pulse is applied to a MESFET, the drain current responds to the stimulus and remains constant during the flat part of the pulse. This, however, is not a sufficient indication that a trap occupancy of the device remains unaltered by the pulse, unless the trap capture time is longer than the pulse rise time. There is a strong evidence presented here that a very fast activation of traps take place while acquiring the I-V points in the saturation region.

CH3577-4/95/0000-1523$01.00 © 1995 IEEE

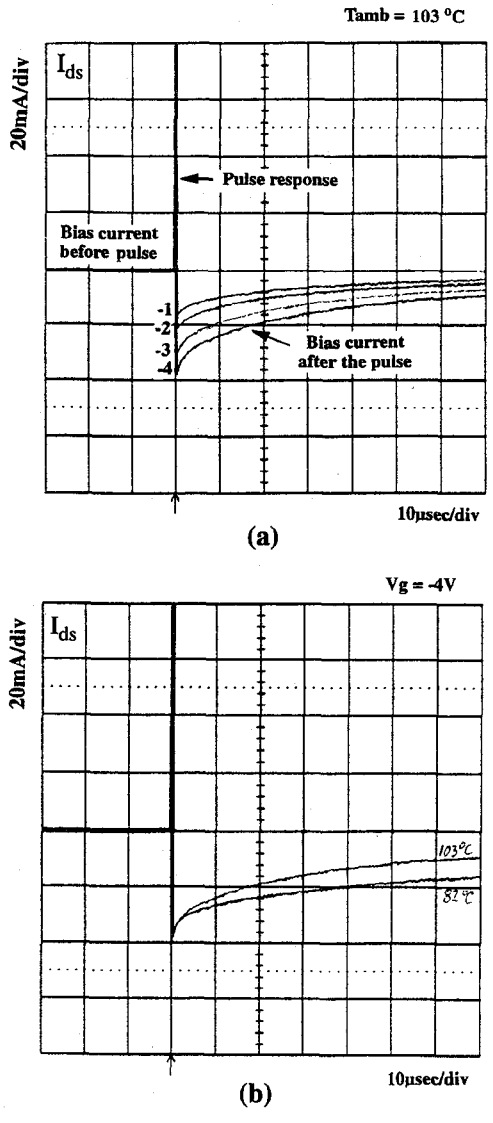

FIGURE 1 Drain bias current response following an application of a large amplitude 40 nanoseconds duration pulse. (a) 6V drain pulse with various gate pulse levels. (b) 6V drain and -4V gate pulse for two different ambient temperatures.

This can be seen in Fig 1 where a 40 nanosecond duration test pulse quite significantly alters occupancy of what is most likely to be the deep level traps in the channel-substrate interface. The resulting back-gating manifests itself in a substantial reduction of drain bias current after the pulse. Trap emission rate and hence time of the return to the pre-pulse bias state is highly temperature dependent and ranges from a few tens of microseconds to a few seconds. This long recovery time (especially at room temperature) is the major limiting factor of the speed with which the dynamic I-V characteristic can be acquired. The interesting thing is that this injection effect is highly dependent on a bias condition. This may be due to alteration of the surface states occupancy by the bias which modifies the electric field distribution in the channel and consequently changes conditions at the channel substrate interface which influence the state of the deep traps. Some insight into this phenomenon may be found in [6]. Estimation of the deep trap effects on I_{ds} is relatively simple. Since these traps activate so quickly, they can easily be distinguished from the surface states and temperature effects by filling them with a very short test pulse. The back-gating of the channel caused by the deep traps can be monitored by measuring the difference in the drain bias current just before and just after the pulse (for non-zero current bias). Acquisition of each pulsed point causes a different amount of trap activation. Therefore, any pulsed measured point and the corresponding amount of bias current reduction due to the deep trap should be treated and displayed as a pair. Making a reasonable assumption that the back-gating reduces the pulsed current by a similar extent as it reduces the bias current (if they are both in the saturation region) we propose a method of displaying the trap effect by showing what the pulsed current would have been if the state of the trap wasn't affected by the pulse. This is done by simply adding a line to the corresponding point whose length is equal to the bias current reduction. The result is shown in Fig 2.

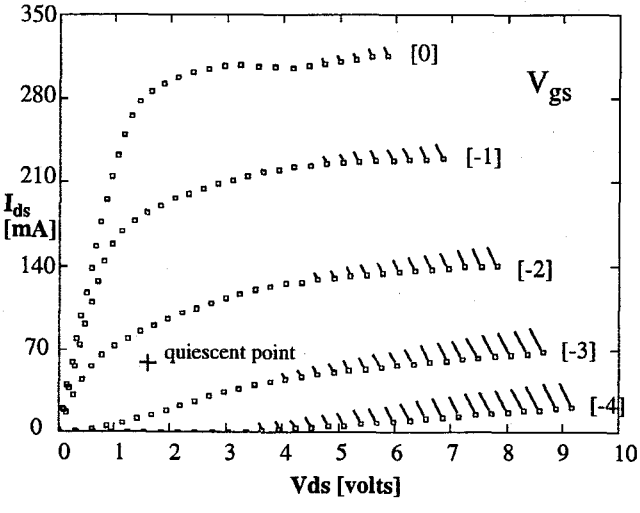

FIGURE 2 Pulsed I-V characteristic (100ns pulse) of HMF-1200 power MESFET with the correction for deep trap effects for each acquired point. Note, that the trap effects can explain the change of slope in the I-V characteristics in the saturation region.

The mapping of the trap provides the explanation for the change of slope in the I-V characteristics in the middle of the saturation region which can also be observed in the data presented in [1] [2].

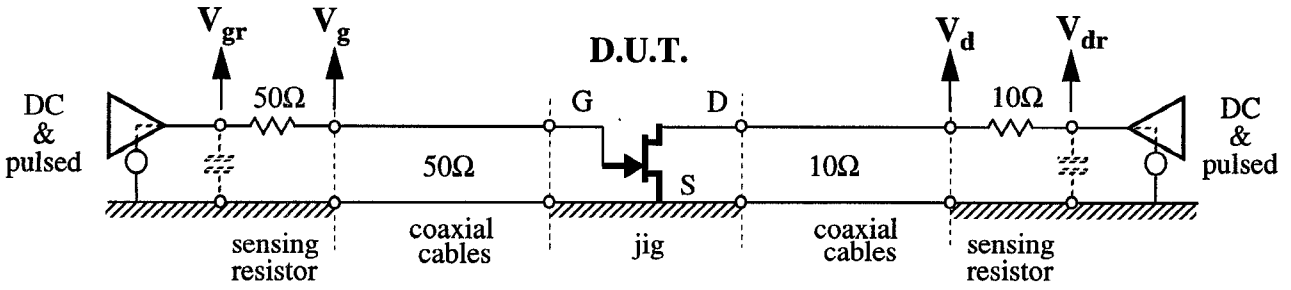

FIGURE 3 Principle of pulsed I-V measurement and the connection between the D.U.T. and the instrumentation

CONNECTION BETWEEN D.U.T. AND INSTRUMENTATION

There is a small but noticeable difference between 100nsec and 200nsec pulsed characteristics. This implies that 100nsec is the longest pulse duration which should be recommended for the pulsed I-V device characterisation. There may even be an advantage in using shorter pulses. However, the shorter the pulse the more difficult it is to control the instantaneous voltages applied at the terminal of the DUT through any length of wire. The most reliable solution in this circumstance is to adopt the configuration shown in Fig 3, where the coaxial cables are utilised and matched at the instrumentation ends. Currents that flow into the device under test are derived from the potential difference across the matching resistors. These resistors also greatly help in controlling breakdown currents. The drain resistor must be large enough to match the impedance of the available coaxial cable and provide a sufficient voltage drop for current sensing and yet be small enough to avoid excessive power dissipation. Any desired voltage can still be applied to the DUT's ports by iterating voltages applied to the resistors.

THERMAL RESPONSE AND TEMPERATURE MEASUREMENTS

Measurement of the device channel temperature is accomplished by utilising the strong dependence on temperature of the voltage across a forward biased Schottky junction of the gate. Normally, a constant current is used to bias the junction, however, this is rather difficult to incorporate in the system in Fig 3. Instead, a 1V potential is applied to the gate sensing resistor which causes a forward current in the range of 3mA to 6mA to flow into the gate. An instant before the forward bias is applied, the drain voltage is switched from its quiescent value to zero for the duration of the test. The resultant V_g (gate potential) can be measured in as little as 200nsec, in which case the device retains its temperature acquired prior to this measurement. This period can be varied by up to 6msec which is usually sufficiently long for the DUT to cool down. This enables the device cooling thermal response to be established. Cooling curves for three different bias points but for the same power delivered to the DUT are presented in Fig 4 .

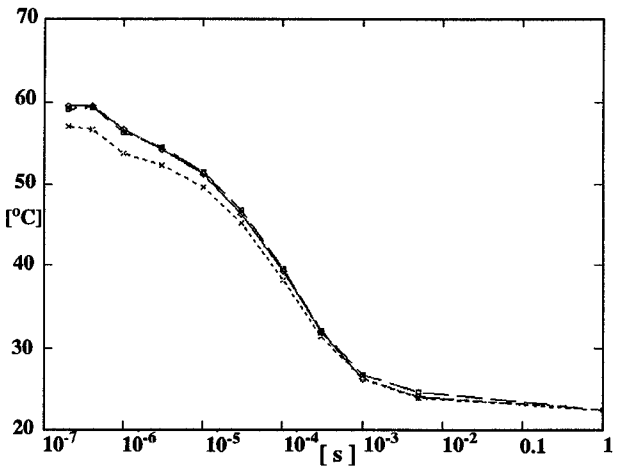

FIGURE 4 Cooling curves for three different bias points but the same 0.5W of power dissipated in the Philips D07M MESFET.

Two of the curves corresponding to bias points in the saturation region almost overlap. The third (dotted) curve, taken with bias in the linear operating region, indicates lower temperatures for the short cooling periods. This is in agreement with what is expected. In the linear region the heat is dissipated over a wide area which includes ohmic areas in the ungated regions of the channel. Therefore, the temperature sensed by the gate must be lower than in the case of bias in the saturation region where the whole power is dissipated under the gate. Due to the variation of GaAs thermoconductivty with temperature, a more precise way

of characterising thermal response is to apply various power level pulses and to measure the DUT's temperature immediately after the pulse.

In order to use V_g as a channel temperature indicator the exact relation between this parameter and the temperature for a given device must be first established. This is done automatically by varying ambient temperature and monitoring Vg with drain bias kept at zero volts (i.e. DUT's internal power dissipation is close to none and hence its temperature must be the same as the ambient temperature). An assumption, verified experimentally, is made here that the trap occupancy alteration caused by changing the quiescent point has an insignificant effect on the relationship between temperature and V_g.

A DEDICATED PULSED I-V SYSTEM

The system is composed of a standard A/D & I/O card plugged into a 386/486 PC computer, in-house developed pulse measurement circuitry, a standard hot plate, and a thermocouple thermometer capable of measuring backplate temperature of the DUT. The DUT is embedded inside a test jig which can be heated up. A computer program FETPULSE, written in C, has been developed to control the system, to automate the execution of various test procedures and to display results. The systems main components and their arrangement is shown in Fig 5.

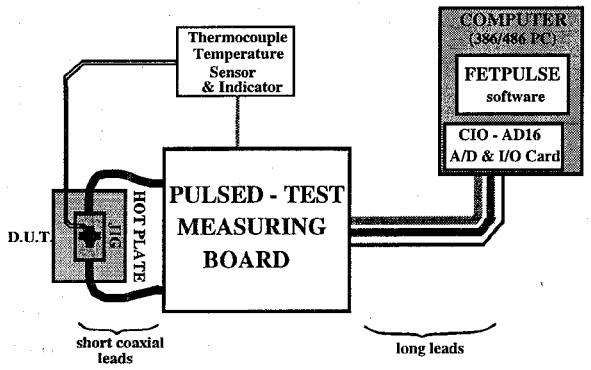

FIGURE 5 Diagram of the system arrangement

Flexibility of the system in terms of test procedure modification is retained by having all the control functions carried out by the computer. The pulsed-test measuring board provides the fast analogue and power requiring functions. Timing of pulse widths and repetition rate come from a timer on the A/D & I/O card, while the precise timing of pulse onset and sampling point is determined by the circuitry on the measuring board. For technical specification and details concerning design and operation of the system see reference [7].

SUMMARY

Low frequency behaviour of microwave FETs is far from being fully understood at present. To gain that understanding and to establish more accurate models for simulation new measuring techniques are required. Techniques of quantifying and distinguishing thermal effect, surface state effects and deep level bulk traps have been established and are presented in this paper.

REFERENCES

[1] S. Pritchett, R. Stewart, J. Mason, G. Brehm, D. Christie, "Precision Pulsed I-V System for Accurate GaAs Device I-V Plane Characterization," IEEE MTT-S Digest, 1994, pp. 1353-1356.

[2] A. Platzker, A. Palevsky, S. Nash, W. Struble, Y. Tajima, "Characterization of GaAs Devices by a Versatile Pulsed I-V Measurement System," IEEE MTT-S Digest, 1990, pp. 1137-1140.

[3] F. Filicori, G. Vannini, A. Mediavilla, A. Tazon, "Modelling of deviations between static and dynamic drain characteristics in GaAs FETs," 23rd EuMC, 1993, September, Madrid, pp. 454-457.

[4] J. Graffeuil, Z. Hadjoub, J. P. Fortea, M. Pouysegur, "Analysis of capacitance and transconductance frequency dispersions in MESFETs for surface characterization," Solid-State Electronics, 1986, Vol. 29, No. 10, pp. 1087-1097.

[5] M. Paggi, P. H. Williams, "Nonlinear GaAs MESFET Modelling Using Pulsed Gate Measurements," IEEE TMTT, Vol. 36, No. 12, December 1988, pp. 1593-1597.

[6] P. H. Ladbrooke, S. R. Blight, "Low-Field Low-Frequency Dispersion of Transconductance in GaAs MESFETs with Implications for Other Rate-Dependent Anomalies," IEEE Transactions on Electron Devices, Vol. 35, No. 3, March 1988, pp. 257-267.

[7] A. K. Jastrzebski, R. J. Donarski, "Pulsed I-V Measurement System For Temperature And Dispersion Characterisation of Microwave FET's," Digest of the 20th ARMMS Meeting, Nottingham, pp. 95-100, March 1994.

[8] A.K.Jastrzebski, "Characterisation aand Mmodelling of Temperarure and Dispertion Effects in Power MESFETs", 24 European Microwave Conference, Canes, pp1319-1324, Sept.11994.